

MICROARCHITECTURE OF AN ARITHMETIC UNIT

Abstract of the Disclosure

The microarchitecture of the arithmetic unit
5 includes two cascaded N bit adders to provide an N bits
result in an accumulator. The arithmetic unit also
includes a carry save adder, followed by an adder,
which, along with the accumulator, are extended to N+1
bits. A circuit for determining the output carry value
10 associated with the result is also provided.

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